has been programmed to the first programming state and the second memory cell has been programmed to the second programming state. The concurrently verifying includes biasing a first bit line connected to the first memory cell to a first bit line voltage while biasing a second bit line connected to the second memory cell to a second bit line voltage different from the first bit line voltage.

[0078] One embodiment of the disclosed technology includes a memory array including a first memory cell and a second memory cell and one or more control circuits configured to identify a first programming state for the first memory cell and identify a second programming state different from the first programming state for the second memory cell. The one or more control circuits configured to store a first voltage based on the first programming state and to store a second voltage different from the first voltage based on the second programming state. The one or more control circuits configured to bias a first bit line connected to the first memory cell to a first bit line voltage based on the first voltage while a second bit line connected to the second memory cell is biased to a second bit line voltage different from the first bit line voltage based on the second voltage. The one or more control circuits configured to sense a first current from the first memory cell while the first bit line is biased to the first bit line voltage and sense a second current from the second memory cell while the second bit line is biased to the second bit line voltage.

[0079] For purposes of this document, it should be noted that the dimensions of the various features depicted in the figures may not necessarily be drawn to scale.

[0080] For purposes of this document, reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "another embodiment" may be used to describe different embodiments and do not necessarily refer to the same embodiment.

[0081] For purposes of this document, a connection may be a direct connection or an indirect connection (e.g., via another part). In some cases, when an element is referred to as being connected or coupled to another element, the element may be directly connected to the other element or indirectly connected to the other element via intervening elements. When an element is referred to as being directly connected to another element, then there are no intervening elements between the element and the other element.

[0082] For purposes of this document, the term "based on" may be read as "based at least in part on."

[0083] For purposes of this document, without additional context, use of numerical terms such as a "first" object, a "second" object, and a "third" object may not imply an ordering of objects, but may instead be used for identification purposes to identify different objects.

[0084] For purposes of this document, the term "set" of objects may refer to a "set" of one or more of the objects.

[0085] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.

What is claimed is:

1. An apparatus, comprising:

a first sense amplifier configured to identify a first programming state for a first memory cell and bias a first bit line connected to the first memory cell to a first bit line voltage based on the first programming state at a first point in time, the first sense amplifier configured to sense a first current from the first memory cell while the first bit line is biased to the first bit line voltage; and

a second sense amplifier configured to identify a second programming state different from the first programming state for a second memory cell and bias a second bit line connected to the second memory cell to a second bit line voltage based on the second programming state at the first point in time, the second sense amplifier configured to sense a second current from the second memory cell while the second bit line is biased to the second bit line voltage.

2. The apparatus of claim **1**, wherein:

the first sense amplifier configured to verify that the first memory cell has been programmed to the first programming state while the first bit line is biased to the first bit line voltage; and

the second sense amplifier configured to verify that the second memory cell has been programmed to the second programming state while the second bit line is biased to the second bit line voltage.

3. The apparatus of claim **1**, wherein:

the first sense amplifier configured to set a first dynamic node associated with the first sense amplifier to a first voltage; and

the second sense amplifier configured to set a second dynamic node associated with the second sense amplifier to a second voltage different from the first voltage.

4. The apparatus of claim **3**, wherein:

the first sense amplifier configured to set a gate of a first NMOS transistor connected to the first bit line to the first voltage; and

the second sense amplifier configured to set a gate of a second NMOS transistor connected to the second bit line to the second voltage.

5. The apparatus of claim **3**, wherein:

the first sense amplifier configured to set the first dynamic node to the first voltage prior to the second dynamic node being set to the second voltage.

6. The apparatus of claim **1**, wherein:

the first bit line voltage is greater than the second bit line voltage.

7. The apparatus of claim **1**, wherein:

the first memory cell corresponds with a first floating-gate transistor; and

the second memory cell corresponds with a second floating-gate transistor.

8. The apparatus of claim **1**, wherein:

the first memory cell corresponds with a first ReRAM memory cell; and

the second memory cell corresponds with a second ReRAM memory cell.

9. The apparatus of claim **1**, wherein:

the first memory cell and the second memory cell are part of a memory array, the memory array comprises a three-dimensional memory array.

10. The apparatus of claim **1**, wherein:

the first memory cell and the second memory cell are part of a memory array, the memory array comprises a non-volatile memory that is monolithically formed in one or more physical levels of memory cells having active areas disposed above a silicon substrate.